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EXAMINER	
MOUTTET, BLAISE L	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,296	EDELEN ET AL.	
	Examiner	Art Unit	
	Blaise L. Mouttet	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,15-26,28,31-44,46 and 49-52* is/are rejected.

7)☒ Claim(s) *11,13,14,27,29,30,45,47 and 48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as follows:

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

23, 24, 26, and 28 as shown in figure 1.

The description of figure 3 appears to indicate that the figure is based on a prior art printhead model (HP57). This figure should be labeled as "PRIOR ART" (or at least "RELATED ART") in accordance with this description.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because of the word "comprises" which is considered legal terminology and improper for a patent abstract.

Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 2, 3, 5, 11, 17, 20, 22-33, 36, 37 and 42-45 are objected to because of the following informalities:

In claims 2, 5, 11, 17, 36, 39, 44, and 45 "the memory element" is recited however since plural memory elements are previously recited this should be more properly stated as --at least one of the memory elements-- or an equivalent.

In claims 13, 14, 47, and 48 "the pnp devices" is recited however antecedent basis is provided for only one pnp device. It is suggested that an intermediate limitation be provided in claims 13, 14, 47, and 48 specifying that there is a plurality of the pnp devices.

In claims 20, 26, and 27 "the fuse element" is recited however no antecedent basis is provided for a fuse element. In light of the specification it is suggested that the fuse element be specified as at least one of the memory elements to overcome this objection.

In claims 22, 23, 31, and 32 "the circuit element" is recited however since plural circuit elements are previously recited this should be more properly stated as --at least one of the circuit elements--.

In claim 23, "..configured to the circuit element.." should read --..configured to isolate the circuit element..-- in accordance with the intended meaning.

In claim 33, "the fuse density" should read --a fuse density-- since this is a new limitation.

In claims 42-45 "the surrounding guard ring" is recited however there is no antecedent basis for this term in claim 40. It is suggested that these claims be amended so as to depend from claim 41 which contains the appropriate antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 16, 35, 36, and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu et al. US 6,568,783 B2.

Hu et al. discloses, regarding claim 1, a programmable memory (75) on an inkjet printhead chip (figure 7), the memory comprising:

a memory array having a plurality of memory elements (fuses 87 in figure 11 and described in column 4, lines 45-56); and

a bipolar device (one of the diodes 88) isolating a memory element (87) from another memory element (87) in the memory array (as explained in column 4, lines 20-25 the bipolar diodes function to isolate separate power supply lines for the separate memory elements and thus also isolate the fuses used as the memory elements).

Regarding claim 2, the memory elements (87) are fuses (figure 11).

Regarding claim 16, the bipolar device (88) is a diode (figure 11).

Hu et al. discloses, regarding claim 35, a method of providing high fuse density in a printhead heater chip comprising:

arranging a plurality of memory elements (87) in a memory array (as discussed in relation to column 4, lines 45-56 and shown in figure 11 the fuses are manufactured on the printhead chip); and

isolating a memory element (87) from another memory element (87) in the memory array with a bipolar device (88) (as explained in column 4, lines 20-25 the bipolar diodes are provided to isolate separate power supply lines for the separate memory elements and thus also isolate the fuses used as the memory elements).

Regarding claim 36, the memory elements (87) are fuses (figure 11).

Regarding claim 50, the bipolar device (88) is a diode (figure 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 4, 15, 19, 21, 31, 32, 35, 36, 38, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Davis US 4,064,493.

Ishinaga et al. discloses, regarding claims 1 and 19, a programmable memory (PROM 5) on an inkjet printhead chip (100) (figure 1, column 2, lines 35-52, column 4, lines 1-10).

Regarding claims 4, 21, and 38, Ishinaga et al. discloses that the memory (5) is formed on a heater chip (100) with plural laminated heaters (ink ejection elements) (column 3, lines 45-57, column 6, lines 24-31).

Ishinaga et al. discloses, regarding claim 35, a method of providing a programmable memory (PROM 5) in a printhead heater chip (100) (column 3, lines 45-57, column 6, lines 24-31).

It is noted that, given the description of Ishinaga et al., broad teachings relevant to PROM, and the circuitry used therein, would also be relevant to one of ordinary skill in the inkjet art because Ishinaga et al. is particularly concerned with PROM placement on inkjet printhead chips (column 2, lines 47-52).

Ishinaga et al. fails to disclose, regarding claims 1, 2, 15, 19, 31, 32, 35, 36, and 49, the conventional PROM architecture in which the PROM includes a plurality of memory elements arranged in columns and rows wherein the memory elements are fuses and a bipolar device that comprises an npn device that isolate the memory devices.

Davis provides details, regarding claims 1, 2, 15, 19, 31, 35, 36, and 49, of a conventional PROM memory with column and row memory cells and explains that fuses are used as memory elements and bipolar npn transistors are isolation elements for the fuses (figure 3, column 2, lines 6-13). Regarding claim 32, the circuit elements are formed as a layered integrated circuit including resistive (i.e. heating) portions (22) (figure 1c, figure 3).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use the conventional PROM configuration as described by Davis for the PROM on the inkjet printhead chip as taught by Ishinaga et al.

The motivation for doing so would have been that this PROM configuration provides advantages of low current during programming, simple production, and efficient size as explained by column 1, lines 39-44 of Davis.

6. Claims 1, 2, 4-6, 12, 19, 21, 22, 28, 32, 35, 36, 38-40, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Duval et al. US 4,112,505.

Ishinaga et al. discloses, regarding claims 1 and 19, a programmable memory (PROM 5) on an inkjet printhead chip (100) (figure 1, column 2, lines 35-52, column 4, lines 1-10).

Regarding claims 4, 21, and 38, Ishinaga et al. discloses that the memory (5) is formed on a heater chip (100) with plural laminated heaters (ink ejection elements) (column 3, lines 45-57, column 6, lines 24-31).

Ishinaga et al. discloses, regarding claim 35, a method of providing a programmable memory (PROM 5) in a printhead heater chip (100) (column 3, lines 45-57, column 6, lines 24-31).

It is noted that, given the description of Ishinaga et al., broad teachings relevant to PROM, and circuitry used therein, would also be relevant to one of ordinary skill in

the inkjet art because Ishinaga et al. is particularly concerned with PROM placement on inkjet printhead chips (column 2, lines 47-52).

Ishinaga et al. fails to disclose, regarding claims 1, 2, 5, 6, 12, 19, 22, 28, 32, 35, 36, 39, and 40, the conventional PROM architecture in which the PROM includes a plurality of memory elements arranged in columns and rows wherein the memory elements are fuses and a bipolar device that comprise pnp floating gate devices that isolate the memory devices wherein the pnp devices are joined at the n-type base.

Duval et al. provides details, regarding claims 1, 2, 5, 6, 12, 19, 22, 28, 35, 36, 39, and 40, of a conventional PROM memory with column and row memory cells and explains that fuses (F9-F14) are used as memory elements, bipolar pnp transistors (85-90) are isolation elements for the fuses, and the memory elements are connected by a floating gate arrangement (figure 6, column 7, line 45 - column 8, line 13). Regarding claims 12, 28, and 46, the gates of the pnp transistors (85-90) are connected at the n-type bases via resistive regions 72, 73, 76, and 77 (figure 6). Regarding claim 32, the circuit elements are formed as a layered integrated circuit including resistive (i.e. heating) portions (22) (figures 8 and 9).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use the conventional PROM configuration as described by Duval et al. for the PROM on the inkjet printhead chip as taught by Ishinaga et al.

The motivation for doing so would have been that this PROM configuration provides advantages of high memory density with reduced manufacturing cost as explained by column 3, lines 13-22 of Duval et al.

7. Claims 3 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. US 6,568,783 B2 in view of Baek US 2004/0085405 A1.

Hu et al. discloses the subject matter of claims 2 and 36 as described in the 35 USC 102 rejection.

Hu et al. fails to disclose that the fuse comprises TaAl or TaAlN.

Baek discloses that TaAl is a preferred material for fuses on inkjet printheads to optimally fuse with the least energy (paragraph [0015], [0027]).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use TaAl as the material for the fuses of Hu et al. as taught by Baek.

The motivation for doing so would have been to minimize energy requirements as taught by paragraph [0015] of Baek.

8. Claims 7, 8, 23, 24, 41, and 42, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Duval et al. US 4,112,505, as applied to claims 6, 19, and 40, and further in view of Oakes US 3,697,828.

Ishinaga et al. in view of Duval et al. render obvious the subject matter of claims 6, 19, and 40 as explained in the 35 USC 103 rejection above.

Ishinaga et al. in view of Duval et al. fail to disclose p-type guard rings positioned around the pnp transistors of the memory to isolate the pnp transistors.

Oakes discloses that p-type guard rings are conventionally employed to isolate pnp transistors (abstract).

It would have been obvious to a person of ordinary skill in the inkjet art at the time of the invention to utilize p-type guards as suggested by Oakes for the pnp transistors of Ishinaga et al. in view of Duval et al.

The motivation for doing so would have been to solve the problem of short circuits efficiently (column 1, lines 13-45, column 2, lines 33-52).

9. Claims 9, 10, 25, 26, 43, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Duval et al. US 4,112,505 and Oakes US 3,697,828, as applied to claims 7, 23, and 41, and further in view of Uchida US 4,723,155.

Ishinada et al. in view of Duval et al. and Oakes render obvious the subject matter of claims 7, 23, and 41 as explained in the 35 USC 103 rejection above.

Ishinda et al. in view of Duval et al. and Oakes are silent as to the positioning of a fuse memory element relative to a guard ring and fails to teach using n-type guards.

Uchida discloses positioning fuses of PROMs within guard rings (fig. 4A, 4B, column 2, lines 7-33) and using a dual structure p-type/n-type guard ring (column 7, lines 25-38).

It would have been obvious for a person of ordinary skill in the art at the time of the invention to position the fuse memory elements of Ishinada et al. in view of Duval et al. and Oakes within a dual n-type/p-type guard ring as taught by Uchida.

The motivation for doing so would have been to increase the reliability of the PROM memory as taught by column1, lines 10-15 and column 2, lines 7-11 of Uchida.

10. Claims 17, 33, 51, and 53 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Duval et al. US 4,112,505 as applied to claims 1, 19, and 35 above, and further in view of Prall et al. US 5,636,172.

Ishinaga et al. in view of Duval et al. render obvious the subject matter of claims 1, 19, and 35 as explained in the 35 USC 103 rejection above.

Ishinaga et al. in view of Duval et al. teach, regarding claims 17, 33, 51, and 53, that a programming transistor (shunt transistor 91) is used to facilitate programming of the PROM (column 3, lines 34-41 of Duval et al.)

Ishinaga et al. in view of Duval et al. fail to teach, regarding claims 17, 33, 51, and 53, any specific memory density for the fuses of the PROM.

Prall et al. notes the conventional desires of fuse density in fabricating memory devices and mention a constraint of a 3 micron pitch (column 1, line 46 – column 2, line 2) and teaches an forming an improved pitch of 1.25 microns (column 4, lines 7-27). It is noted that either a 3 micron pitch (333 fuses/millimeter) or 1.25 micron pitch (800 fuses/millimeter) are above the claimed range of a fuse density producing 200 bits/millimeter).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to provide a fuse pitch as taught by Prall et al. producing a memory

density of greater than 200 fuses/millimeter for the programmable memory on the printhead chip of Ishinaga et al. in view of Duval et al.

The motivation for doing so would have been that the memory of printhead chips requires a large memory density (as evidenced at least by column 3, lines 58-65 of Ishinaga et al.) and Prall et al. provides a solution to producing the desirable high memory density.

11. Claims 18, 34, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Duval et al. US 4,112,505 as applied to claims 1, 19, and 35 above, and further in view of Baek US 2004/0085405 A1 and Fujita et al. US 6,733,100 B1.

Ishinaga et al. in view of Duval et al. render obvious the subject matter of claims 1, 19, and 35 as explained in the 35 USC 103 rejection above.

Ishinaga et al. in view of Duval et al. fail to disclose the number of fuses or the resistance of the fuses.

Baek discloses a programmable memory on an inkjet printhead chip (paragraph [0014]) comprising fuses having resistances greater than 5 ohms (paragraph [0060]).

Fujita et al. discloses the requirements for memory on an inkjet printhead and notes the capacity of 1 kbit (1000 bits which requires 1000 memory elements) (column 14, line 61 – column 15, line 21).

It would have been obvious to a person of ordinary skill in the inkjet art at the time of the invention to provide the fuses of Ishinaga et al. in view of Duval et al. to be greater than 5 ohms as suggested by Baek.

The motivation for doing so would have been to avoid the problem of inadvertent fusing caused by noise when the fuse resistance is too low and to keep printhead size small as explained in paragraphs [0017] and [0018] of Baek.

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use at least 128 memory elements to store at least 128 bits of data as suggested by Fujita et al. in the memory of Ishinaga et al. in view of Duval et al. and Baek.

The motivation for doing so would have been to have enough memory in order to store information necessary for error correction, printhead identification, and other pertinent data as cited in column 14, line 61 – column 15, line 21 of Fujita et al.

12. Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga et al. US 6,243,109 B1 in view of Davis US 4,064,493, as applied to claim 19, and further in view of Baek US 2004/0085405 A1.

Ishinaga et al. in view of Davis render obvious the subject matter of claim 19 described in the 35 USC 103 rejection.

Ishinaga et al. in view of Davis fail to disclose that the fuses of the PROM comprise TaAl or TaAlN.

Baek discloses that TaAl is a preferred material for fuses on memory devices of inkjet printheads to optimally fuse with the least energy (paragraph [0015], [0027]).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use TaAl as the material for the fuses of Ishinaga et al. in view of Davis as taught by Baek.

The motivation for doing so would have been to minimize energy requirements as taught by paragraph [0015] of Baek.

13. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baek US 2004/0085405 A1 in view of Fujita et al. US 6,733,100 B1.

Baek discloses a programmable memory on an inkjet printhead chip (paragraph [0014]), the memory comprising:

memory elements (fuses 206) having resistances greater than 5 ohms (paragraph [0060]).

Baek fails to disclose the number of memory elements used.

Fujita et al. discloses the requirements for memory on an inkjet printhead and notes the capacity of 1 kbit (1000 bits which requires 1000 memory elements) (column 14, line 61 – column 15, line 21).

It would have been obvious for a person of ordinary skill in the inkjet art at the time of the invention to use at least 128 memory elements to store at least 128 bits of data as suggested by Fujita et al. in the memory of Baek.

The motivation for doing so would have been to have enough memory in order to store information necessary for error correction, printhead identification, and other pertinent data as cited in column 14, line 61 – column 15, line 21 of Fujita et al.

Allowable Subject Matter

14. Claims 11, 13, 14, 27, 29, 30, 45, 47, and 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and provided the noted formal objections are corrected.

The prior art of record fails to provide sufficient teaching or motivation to one of ordinary skill in the inkjet art to provide the additionally recited features of these claims in the combinations as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Blaise Mouttet who may be reached at telephone number (571) 272-2150. The examiner can normally be reached on Monday-Friday from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier, Art Unit 2853, can be reached at (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Blaise Mouttet March 04, 2005

Blaise Mouttet 03/04/2005

LAMSON NGUYEN
PRIMARY EXAMINER

03/07/05